IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Lawrence W. Yonge III et al.   Art Unit : 2663
Serial No. : 09/632,597   Examiner : Kwoh, J.
Filed   : August 4, 2000
Title   : SEGMENT BURSTING WITH PRIORITY PRE-EMPTION AND REDUCED
            LATENCY

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Technology Center 2600

Commissioner for Patents
Washington, D.C. 20231

RESPONSE

In response to the action mailed July 3, 2002, please amend the application as follows:

In the specification:

Please replace the paragraph beginning at page 8, line 16 with the following rewritten paragraph:

-- During a data transmit process, data and control information are received at the PHY-to-MAC interface (MAC interface) 74 over the PHY-to-MAC bus 24. The MAC interface provides the data to the scrambler 32, which ensures that the data as presented to the input of the data FEC encoder 34 are substantially random in pattern. The data FEC encoder 34 encodes the scrambled data pattern in a forward error correction code and subsequently interleaves the encoded data. Any forward error correction code, for example, a Reed-Solomon, or both a Reed-Solomon code and a convolution code, can be used for this purpose. The modulator 36 reads the FEC encoded data and FEC encoded control information from the frame control FEC encoder 38, and modulates the encoded data and control information onto carriers in OFDM symbols in accordance with conventional OFDM modulation techniques. Those modulation techniques may be coherent or differential. The modulation mode or type may be Binary Phase Shift Keying with 1/2 rate coding ("1/2 BPSK"), Quadrature Phase Shift Keying with 1/2 rate coding

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